What is claimed is:

1. An input circuit comprising:

a data input means for the input of input data;

a data latch means for latching the input data;

a reset means for resetting the data latch means;

a clock synchronization means for synchronizing the input of the input data to the data input means; and

a latch enhancement means for blocking feedthrough current by functioning complementarily to the reset means, and enhancing the latching operation of the data latch means.

2. An input circuit comprising:

a data input means for the input of input data;

a data latch means for latching the input data;

a reset means for resetting the data latch means;

a clock synchronization means for blocking feedthrough current by functioning complementarily to the reset means and synchronizing the input of the input data to the data input means; and

a latch enhancement means for enhancing the latching operation of the data latch means.

3. An input circuit comprising:

a data input means for the input of input data;

a data latch means that provides a combined function of blocking feedthrough current in the reset state and synchronizing the latch of the input data;

a reset means for resetting the data latch means; and

a latch enhancement means for enhancing the latching operation of the data latch means.

4. The input circuit of claim 1, wherein the data latch means has a configuration in which the sources of a first PMOS transistor and a second PMOS transistor are connected to a first power source; the drains of the first PMOS transistor and a first NMOS transistor, and the gates of the second PMOS transistor and a second NMOS transistor are connected to a second output terminal; the drains of the second PMOS transistor and the second NMOS transistor and the gates of the first PMOS transistor and the first NMOS transistor are connected to a first output terminal; the source of the first NMOS transistor is connected to a first common terminal at which one of a pair of complementary signals constituting the input data appears; and the source of the second NMOS transistor is connected to a second common terminal at which the other one of the pair of complementary signals constituting the input data appears.

5. The input circuit of claim 1, wherein the reset means includes the sources of a third PMOS transistor and a fourth PMOS transistor being connected to the first power source; the drain of the third PMOS transistor being connected to the first output terminal; the drain of the fourth PMOS transistor being connected to the second output terminal; and the gates of the third PMOS transistor and the fourth PMOS transistor being

connected to a first clock input terminal.

6. The input circuit of claim 1, wherein the data input means includes a third NMOS transistor being connected to a first data input terminal; the gate of a fourth NMOS transistor being connected to a second data input terminal; the drain of the third NMOS transistor being connected to the first common terminal; the drain of the fourth NMOS transistor being connected to the second common terminal; and the sources of the third NMOS transistor and the fourth NMOS transistor being connected to a third common terminal to which power is supplied from a second power source.

7. The input circuit of claim 1, wherein the clock synchronization means includes the gate of a fifth NMOS transistor being connected to the first clock input terminal; the drain of the fifth NMOS transistor being connected to the third common terminal; and the source of the fifth NMOS transistor being connected to the second power source.

8. The input circuit of claim 1, wherein the latch enhancement means includes the gates of a sixth NMOS transistor and a seventh NMOS transistor being connected to a second clock input terminal; the sources of the sixth NMOS transistor and the seventh NMOS transistor being connected to the second power source; the drain of the sixth NMOS transistor being connected to the output end of the current path of a first

feedthrough-current blocking means; the drain of the seventh NMOS transistor being connected to the output end of the current path of a second feedthrough-current blocking means; the input end of the current path of the first feedthrough-current blocking means being connected to the first common terminal; the input end of the current path of the second feedthrough-current blocking means being connected to the second common terminal; and the control terminals of both the first and second feedthrough-current blocking means being connected to the first clock input terminal.

9. The input circuit of claim 1, wherein the first and second feedthrough-current blocking means includes the gates of both an eighth NMOS transistor and a ninth NMOS transistor being connected to the first clock input terminal; the drain of the eighth NMOS transistor being connected to the first common terminal; the drain of the ninth NMOS transistor being connected to the second common terminal; the source of the eighth NMOS transistor being connected to the drain of the sixth NMOS transistor; and the source of the ninth NMOS transistor being connected to the drain of the seventh NMOS transistor.

10. The input circuit of claim 2, wherein the data input means includes the sources of both a tenth NMOS transistor and an eleventh NMOS transistor being connected to the second power source; the gate of the tenth NMOS transistor being connected to a first data input terminal; the gate of the eleventh NMOS

transistor being connected to a second data input terminal; the drain of the tenth NMOS transistor being connected to a third common terminal at which one of a pair of complementary signals constituting the input data appears; the drain of the eleventh NMOS transistor being connected to a fourth common terminal at which the other one of the pair of complementary signals constituting the input data appears.

11. The input circuit of claim 2, wherein the clock synchronization means includes the gates of twelfth NMOS transistor and thirteenth NMOS transistor being connected to the first clock input terminal; the source of the twelfth NMOS transistor being connected to a third common terminal at which one of a pair of complementary signals constituting the input data appears; the source of the thirteenth NMOS transistor being connected to a fourth common terminal at which the other one of the pair of complementary signals constituting the input data appears; the drain of the twelfth NMOS transistor being connected to a first common terminal; and the drain of the thirteenth NMOS transistor being connected to a second common terminal.

12. The input circuit of claim 2, wherein the latch enhancement means includes the sources of both a fourteenth NMOS transistor and a fifteenth NMOS transistor being connected to a second power source; the gates of both the fourteenth NMOS transistor and the fifteenth NMOS transistor being connected to a second clock input terminal; the drain of the fourteenth

NMOS transistor being connected to a third common terminal at which one of a pair of complementary signals constituting the input data appears; and the drain of the fifteenth NMOS transistor being connected to a fourth common terminal at which the other one of the pair of complementary signals constituting the input data appears.

13. The input circuit of claim 3, wherein the data latch means includes the sources of both a first PMOS transistor and a second PMOS transistor being connected to a first power source; the drain of the first PMOS transistor, the gates of the second PMOS transistor and the nineteenth NMOS transistor, and the input end of the current path of a first clock-synchronization feedthrough-current blocking means being connected to a second output terminal; the gate of the first PMOS transistor, the drain of the second PMOS transistor, the gate of the eighteenth NMOS transistor, and the input end of the current path of a second clock-synchronization feedthrough-current blocking means being connected to a first output terminal; the drain of the eighteenth NMOS transistor being connected to the output end of the current path of the first clock-synchronization feedthrough-current blocking means; the drain of the nineteenth NMOS transistor being connected to the output end of the current path of the second clock-synchronization feedthrough-current blocking means; the source of the eighteenth NMOS transistor being connected to a third common terminal at which one of a pair of complementary signals constituting input data appears; the source of the

nineteenth NMOS transistor being connected to a fourth common terminal at which the other one of the pair of complementary signals constituting input data appears; and the control terminal of the first clock-synchronization feedthrough-current blocking means being connected to the first clock input terminal.

14. The input circuit of claim 13, wherein the first clock-synchronization feedthrough-current blocking means includes the drain of a sixteenth NMOS transistor being connected to a first input end; the gate of the sixteenth NMOS transistor being connected to a third input end; and the source of the sixteenth NMOS transistor being connected to a first output end; and the second clock-synchronization feedthrough-current blocking means includes the drain of a seventeenth NMOS transistor being connected to a second input end; the gate of the seventeenth NMOS transistor being connected to a fourth input end; and the source of the seventeenth NMOS transistor being connected to a second output end.